AMENDMENTS TO THE CLAIMS:

The following is a listing of pending claims (none of which are amended by this document):

1. (Previously Presented) A computer program product comprising instructions which are stored in a memory and which, upon execution by a processor, perform steps of:

generating an admittance matrix for an electrical circuit which is being analyzed, the admittance matrix including symbolic expressions rather than numerical expressions for at least some components of the electrical circuit;

linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electrical circuit, the step of solving the equation system further comprising:

(a) rearranging equations in the equation system;

(b) partitioning the admittance matrix into partitions;

(c) generating a simplified equation system based on the partitioning of step (b).

2. (Previously Presented) The computer program product of claim 1, further comprising linearly and algebraically solving the equation system including the admittance matrix for one of (1) determining a transfer function between specified nodes of the electrical circuit; (2) optimizing a component of the electrical circuit; (3) perturbation/sensitivity analysis, and (4) general circuit design.

3. (Original) The computer program product of claim 1, wherein the electrical circuit has a telecommunications component including one of a multi-winded transformer, a loading coil, a line-driver, an analogue cable, and a filter.

4. (Original) The computer program product of claim 1, wherein the admittance matrix comprises admittance blocks for each of plural subcircuits.

5. (Previously Presented) The computer program product of claim 4, wherein the admittance blocks for the plural subcircuits are situated on a main diagonal of the admittance matrix, and wherein differing types of connectivity blocks which represent connectivity between the plural subcircuits are situated are symmetrically with respect to one another across the main diagonal of the admittance matrix.

6. (Previously Presented) The computer program product of claim 1, wherein step (a) of rearranging the equations in the equation system is performed in accordance with an identification of interesting nodes for analysis; and wherein step (b) of partitioning the admittance matrix into the partitions is performed in accordance with the identification of interesting nodes for analysis.

7. (Original) The computer program product of claim 6, further comprising as step (b) recursively partitioning the admittance matrix into partitions accordance with the identification of interesting nodes for analysis.

8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Cancelled)
14. (Cancelled)

15. (Previously Presented) A computer program product comprising instructions which are stored in a memory and which, upon execution by a processor, perform steps of:

generating an admittance matrix for an electrical circuit which is being analyzed by:

generating a main circuit admittance block for a main circuit comprising the electrical circuit which is being analyzed;

generating a subcircuit admittance block for a subcircuit comprising the electrical circuit which is being analyzed;

inserting the main circuit admittance block and the subcircuit admittance block on a main diagonal of the admittance matrix;

generating plural types of connectivity blocks which represent connectivity between the main circuit and the subcircuit;

inserting the plural types of connectivity blocks so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix;

using the admittance matrix for analyzing at least a part of the electrical circuit.

16. (Original) The computer program product of claim 15, wherein the step of generating the subcircuit admittance block for the subcircuit comprises:

generating a subblock for the subcircuit;

generating an internal voltage subblock for the subcircuit; and

generating a surface connectivity subblock for the subcircuit.

17. (Original) The computer program product of claim 15, wherein the step of generating the subblock for the subcircuit comprises generating one of an impedance subblock, a chain matrix equation, and a scattering matrix.

18. (Previously Presented) The computer program product of claim 15, wherein the step of generating connectivity blocks comprises:

generating a current exchange connectivity block which describes how currents are exchanged between the main circuit and the subcircuit;

generating a voltage potential connectivity block which describes voltages at common nodes between the main circuit and the subcircuit;

inserting the current exchange connectivity block and the voltage potential connectivity block on opposite sides of the main diagonal of the admittance matrix.

19. (Original) The computer program product of claim 15, further comprising using the admittance matrix for one of (1) determining a transfer function between specified nodes of the electrical circuit; (2) optimizing a component of the electrical circuit; (3) perturbation/sensitivity analysis, and (4) general circuit design.

20. (Original) The computer program product of claim 15, wherein the subcircuit comprises one of a multi-winded transformer, a loading coil, a line-driver, an analogue cable, and a filter.

21. (Previously Presented) A method of analyzing an electric circuit comprising:

using a computer to generate an admittance matrix for the electrical circuit, the admittance matrix including symbolic expressions rather than numerical expressions for at least some components of the electrical circuit;

using the computer for linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electrical circuit, the solving of the equation system including the steps of:

(a) rearranging equations in the equation system;

(b) partitioning the admittance matrix into partitions;

(c) generating a simplified equation system based on the partitioning of step (b), and

(d) solving the simplified equation system.

22. (Original) The method of claim 21, further comprising linearly and algebraically solving the equation system including the admittance matrix for one of (1) determining a transfer function between specified nodes of the electrical circuit; (2) optimizing a component of the electrical circuit; (3) perturbation/sensitivity analysis, and (4) general circuit design.

23. (Original) The method of claim 21, wherein the electrical circuit has a telecommunications component including one of a multi-winded transformer, a loading coil, a line-driver, an analogue cable, and a filter.

24. (Original) The method of claim 21, wherein the admittance matrix comprises admittance blocks for each of plural subcircuits.

25. (Previously Presented) The method claim 21, further comprising situating the admittance blocks for the plural subcircuits on a main diagonal of the admittance matrix, and situating differing types of connectivity blocks which represent connectivity between the plural subcircuits symmetrically with respect to one another across the main diagonal of the admittance matrix.

26. (Previously Presented) The method claim 21, wherein step (a) comprises rearranging the equations in the equation system in accordance with an identification of interesting nodes for analysis; and wherein step (b) comprises partitioning the admittance matrix into the partitions accordance with the identification of interesting nodes for analysis.

27. (Original) The method claim 26, further comprising as step (b) recursively partitioning the admittance matrix into partitions in accordance with the identification of interesting nodes for analysis.

28. (Cancelled)
29. (Cancelled)
30. (Cancelled)
31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Previously Presented) A method of analyzing an electric circuit comprising:

using a computer to generate an admittance matrix for the electrical circuit by:

generating a main circuit admittance block for a main circuit comprising the electrical circuit which is being analyzed;

generating a subcircuit admittance block for a subcircuit comprising the electrical circuit which is being analyzed;

inserting the main circuit admittance block and the subcircuit admittance block on a main diagonal of the admittance matrix;

generating plural types of connectivity blocks which represent connectivity between the main circuit and the subcircuit;

inserting the plural types of connectivity blocks so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix;

using the admittance matrix for analyzing at least a part of the electrical circuit.

36. (Original) The method of claim 35, wherein generating the subcircuit admittance block for the subcircuit comprises:

generating a subblock for the subcircuit;

generating an internal voltage subblock for the subcircuit; and

generating a surface connectivity subblock for the subcircuit.

37. (Original) The method of claim 35, wherein the step of generating the subblock for the subcircuit comprises generating one of an impedance subblock, a chain matrix equation, and a scattering matrix.

38. (Previously Presented) The method of claim 35, wherein the step of generating connectivity blocks comprises:

generating a current exchange connectivity block which describes how currents are exchanged between the main circuit and the subcircuit;

generating a voltage potential connectivity block which describes voltages at common nodes between the main circuit and the subcircuit;

inserting the current exchange connectivity block and the voltage potential connectivity block on opposite sides of the main diagonal of the admittance matrix.

39. (Original) The method of claim 35, further comprising using the admittance matrix for one of (1) determining a transfer function between specified nodes of the electrical circuit; (2) optimizing a component of the electrical circuit; (3) perturbation/sensitivity analysis, and (4) general circuit design.

40. (Original) The method of claim 35, wherein the subcircuit comprises one of a multi-winded transformer, a loading coil, a line-driver, an analogue cable, and a filter.